

-100mA / -50V Digital transistor (with built-in resistor)

DTA113TKA

●Applications

Inverter, Interface, Driver

●Features

- 1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors.
- 2) The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input, and parasitic effects are almost completely eliminated.
- 3) Only the on/ off conditions need to be set for operation, making the device design easy.
- 4) Higher mounting densities can be achieved.

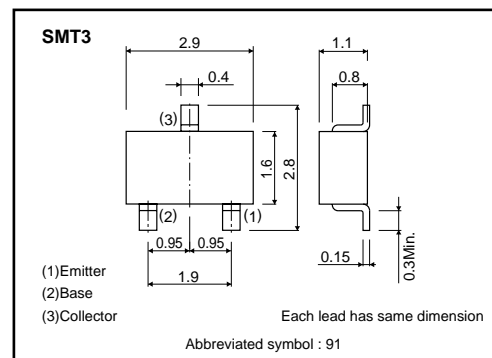
●Structure

PNP epitaxial planar silicon transistor
(Resistor built-in type)

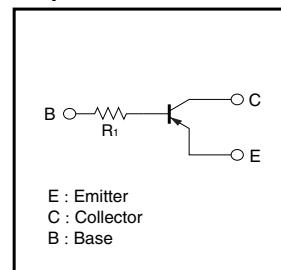
●Packaging specifications

Part No.	Package	SMT3
	Packaging type	Taping
	Code	T146
	Basic ordering unit (pieces)	3000
DTA113TKA		○

●External dimensions (Unit : mm)



●Equivalent circuit



$R_1=1k\Omega$

●Absolute maximum ratings ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Collector-base voltage	V_{CB0}	-50	V
Collector-emitter voltage	V_{CE0}	-50	V
Emitter-base voltage	V_{EB0}	-5 to +10	V
Collector current	I_c	-100	mA
Collector Power dissipation	P_c	200	mW
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Transistors

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV_{CBO}	-50	-	-	V	$I_C = -50\mu A$
Collector-emitter breakdown voltage	BV_{CEO}	-50	-	-	V	$I_C = -1mA$
Emitter-base breakdown voltage	BV_{EBO}	-5	-	-	V	$I_E = -50\mu A$
Collector cutoff current	I_{CBO}	-	-	-0.5	μA	$V_{CB} = -50V$
Emitter cutoff current	I_{EBO}	-	-	-0.5	μA	$V_{EB} = -4V$
Collector-emitter saturation voltage	$V_{CE(sat)}$	-	-	-0.3	V	$I_C/I_B = -5mA / -0.25mA$
DC current transfer ratio	h_{FE}	100	250	600	-	$I_C = -1mA, V_{CE} = -5V$
Input resistance	R_1	0.7	1	1.3	$k\Omega$	-
Transition frequency	f_T *	-	250	-	MHz	$V_{CB} = -10V, I_E = 5mA, f = 100MHz$

* Characteristics of built-in transistor

●Electrical characteristics curves

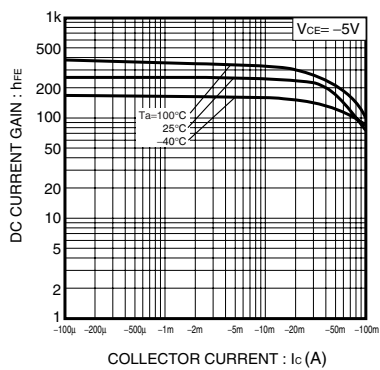


Fig.1 DC Current gain vs. Collector Current

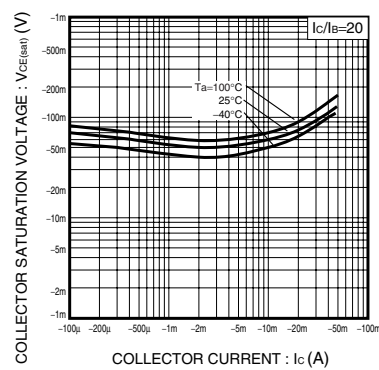


Fig.2 Collector-emitter saturation voltage vs. Collector Current

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